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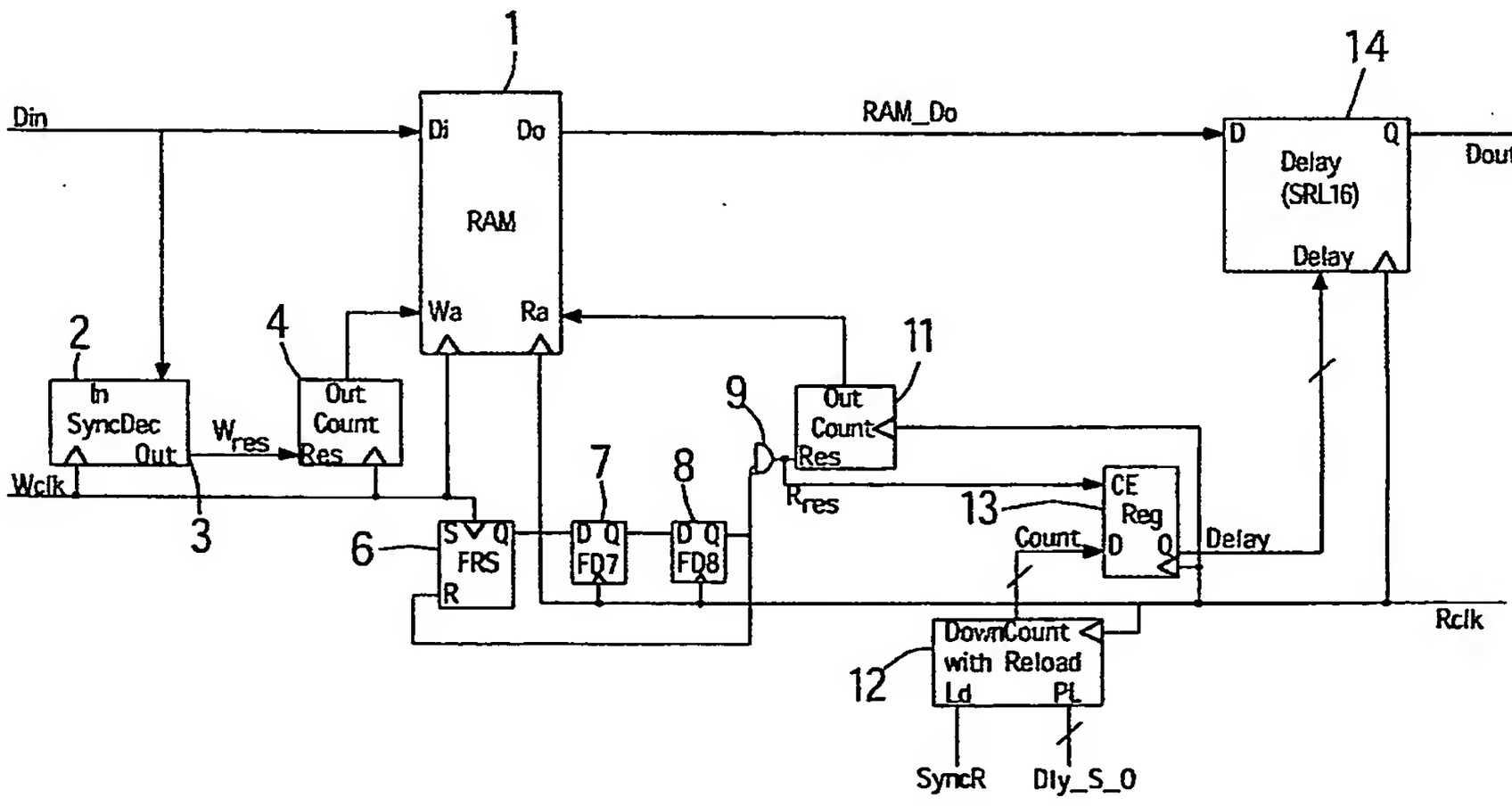
(54) Title: CIRCUIT FOR ADDRESSING A MEMORY



(57) Abstract: A circuit is proposed which has a memory to which input data can be written at different write addresses with a first clock rate and from which output data can be read at different read addresses with a second clock rate. The memory can be fed a write reset pulse that resets the write address to an initial value. In addition, the memory can be fed a read reset pulse by means of which the data are output in a fixed temporal relationship. Finally, the circuit proposed is provided with switching means in order to derive the read reset pulse from the write reset pulse. This ensures that the two reset pulses cannot occur simultaneously.

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